§103(a) as being unpatentable over U.S. Patent No. 5,361,685 to Tanaka in view of U.S. Patent No. 6,130,311 to Kurz et al. ("Kurz"). Claims 21-24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tanaka. Claims 4-11 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,247,277 to Mori et al. ("Mori") in view of Kurz. Claims 1, 3, 25 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,489,062 to Watanabe et al. ("Watanabe"). Claims 26-29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watanabe in view of Tanaka.

In accordance with the present response, the specification has been suitably revised to correct informalities, provide antecedent basis for the claim language, and place it in better conformance with U.S. practice. The title of the invention has been changed to "METHOD OF PRODUCING ELECTRICAL DOUBLE LAYER CAPACITOR AND METHOD OF MOUNTING ELECTRICAL DOUBLE LAYER CAPACITOR ON A CIRCUIT SUBSTRATE" to more clearly reflect the invention to which the amended and new claims are directed. Original independent claims 1 and 4 have been amended to further patentably distinguish from the prior art of record. Claims 4-11 have also been amended to overcome the indefiniteness rejection raised by the Examiner. Claims 1-11 have also been amended in formal respects to improve the wording thereof.

Non-elected claims 12-20, 31 and 32 have been canceled without prejudice or admission and subject to applicants' right to file a continuing application to pursue the subject matter of the non-elected claims. Claims 21-30 have been canceled without prejudice or admission, thereby rendering the indefiniteness and prior art rejections of these claims moot. New claims 33-55 have been added to provide a fuller scope of coverage. A new abstract which more clearly reflects the invention to which the amended and new claims are directed has been substituted for the original abstract.

In view of the foregoing, applicants respectfully submit that the rejection of claims 4-11 under 35 U.S.C. §112, second paragraph, has been overcome and should be withdrawn.

Attached hereto is a marked-up version of the changes made to the title, abstract, specification and claims by the current amendment. The attached pages i-ix are captioned **"VERSION WITH MARKINGS TO SHOW CHANGES MADE."**

Applicants respectfully request reconsideration of their application in light of the following discussion.

Brief Summary of the Invention

The present invention is directed to a method of producing an electrical double layer capacitor and to a method of mounting the electrical double layer capacitor on a circuit substrate.

Conventional coin- or button-type electrical double layer capacitors which are mounted on a circuit board by reflow soldering utilize an organic solvent for the electrolyte, a metallic oxide for the positive electrode, and a negative electrode containing lithium to provide the active material. In such conventional capacitors, the components are active by nature. Accordingly, if the quantity ratio of the components changes depending on the fluctuation in the production process, such a change could cause bulging and/or liquid leakage (e.g., leaking of the electrolyte to the outside of the capacitors) during reflow soldering when the capacitors are mounted on the circuit board.

Furthermore, the adequate performance of electrical double layer capacitors mounted by reflow soldering must be assured after reflow soldering. However, there are some cases in which the capacitors contain a large amount of foreign substances (e.g., water). At room temperature, the characteristics of such capacitors are not influenced. However, after reflow soldering or after storage of such capacitors, a sudden deterioration occurs in the characteristics of such capacitors.

The present invention overcomes the drawbacks of the conventional art. Figs. 1-2 show an embodiment of an electrical double layer capacitor produced by the method

according to the present invention embodied in the claims. A a positive electrode 101, a negative electrode 104, a non-aqueous solvent 102, an electrolyte 109 containing a supporting salt, a separator 108, and a gasket 107 are assembled together to form an electrical double layer capacitor (e.g., of a coin- or button-type). The assembled electrical double layer capacitor is then heated. In one embodiment, the heating step comprises heating the assembled electrical double layer capacitor at a temperature in a range of 180 to 300 °C.

In another aspect, the present invention is directed to a method of mounting an electrical double layer capacitor on a circuit substrate. With reference to Fig. 1, a positive electrode 101, a negative electrode 104, a non-aqueous solvent 102, an electrolyte 109 containing a supporting salt, a separator 108, and a gasket 107 are assembled together to form an electrical double layer capacitor (e.g., of a coin- or button-type). The assembled electrical double layer capacitor is then heated. Thereafter, the heated assembled electrical double layer capacitor is arranged on a circuit substrate and reflow soldered.

In one embodiment, a temperature profile of the heating step in a heating region under 150 °C is within a range of 50% to 150% of a temperature profile of the reflow

soldering step in the heating region under 150 °C. In another embodiment, a duration of the heating step in a heating region under 150°C is within a range of 50% to 150% of a duration of the reflow soldering step in the heating region under 150°C.

By the foregoing methods according to the present invention embodied in the claims, foreign substances (e.g., water) contained in the assembled electrical double layer capacitor are removed during the heating step which is conducted prior reflow soldering. Additionally, bulging and liquid leakage (e.g., leaking of the electrolyte to the outside of the capacitor) during reflow soldering are prevented when the capacitor is mounted on the circuit board.

The prior art of record does not disclose or suggest the subject matter recited in amended claims 1-11 and newly added claims 33-53.

Traversal of Prior Art Rejections

Claims 1-3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Kurz. Applicants respectfully traverse this rejection and submit that the combined teachings of Tanaka and Kurz do not disclose or suggest the subject matter recited in amended claims 1-3.

Amended independent claim 1 is directed to a method for producing an electrical double layer capacitor and

requires the steps of assembling together components comprised of a positive electrode, a negative electrode, a non-aqueous solvent, an electrolyte containing a supporting salt, a separator, and a gasket to form a coin- or button-type electrical double layer capacitor, and heating the assembled coin- or button-type electrical double layer capacitor. No corresponding combination of steps are disclosed or suggested by the prior art of record.

The primary reference to Tanaka discloses a method in which a positive electrode, a negative electrode, and a non-aqueous electrolyte are assembled together to form a non-aqueous battery. As recognized by the Examiner, Tanaka does not disclose or suggest the assembly of an electrical double layer capacitor and a step of heating the assembled double layer capacitor, as required by amended independent claim 1.

The Examiner cited the secondary reference to Kurz for its disclosure of polyester films used to produce film capacitors. In Kurz, the polyester films are heat-treated for the purpose of ensuring the heat stability of the polyester films and the soldering-bath stability of the resulting capacitors (col. 1, lines 25-29). However, Kurz does not disclose or suggest a step of heating a capacitor after the capacitor has been assembled (e.g., assembled using the polyester films), as required by amended independent claim 1.

In Kurz, the heating step during fabrication of the capacitor corresponds to heat-treatment of the polyester films (see examples and comparative examples in columns 5-6), not to a step of heating the assembled capacitor.

Since Kurz does not disclose or suggest a step of heating a capacitor after the capacitor has been assembled, as required by amended independent claim 1, it does not cure the deficiencies of Tanaka. Accordingly, one ordinarily skilled in the art would not have been led to modify the references to attain the claimed subject matter.

Claims 2-3 depend on and contain all of the limitations of amended independent claim 1 and, therefore, distinguish from the references at least in the same manner as claim 1.

In view of the foregoing, applicants respectfully request that the rejection of claims 1-3 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Kurz be withdrawn.

Claims 4-11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Mori in view of Kurz. Applicants respectfully traverse this rejection and submit that the combined teachings of Mori and Kurz do not disclose or suggest the subject matter recited in amended claims 4-11.

Amended independent claim 4 is directed to a method of mounting an electrical double layer capacitor on a circuit substrate and requires the steps of providing a circuit substrate, and assembling together components comprised of a positive electrode, a negative electrode, a non-aqueous solvent, an electrolyte containing a supporting salt, a separator, and a gasket to form a coin- or button-type electrical double layer capacitor. Amended claim 4 further requires heating the assembled coin- or button-type electrical double layer capacitor, arranging the heated assembled coin- or button-type electrical double layer capacitor on the circuit substrate, and reflow soldering the heated assembled coin- or button-type electrical double layer capacitor on the circuit substrate. No corresponding combination of steps is disclosed or suggested by the prior art of record.

The primary reference to Mori discloses a method in which a positive electrode, a negative electrode, an electrolyte, and a gasket are assembled together to form an organic electrolyte battery. As recognized by the Examiner, Mori does not disclose or suggest the assembly of an electrical double layer capacitor and a step of heating the assembled double layer capacitor, as required by amended independent claim 4.

The Examiner cited the secondary reference to Kurz for its disclosure of polyester films used to produce film capacitors. However, Kurz does not disclose or suggest a step of heating a capacitor after the capacitor has been assembled, as required by amended independent claim 1, as set forth above for the rejection of claims 1-3 under 35 U.S.C. §103(a). Since Kurz does not disclose or suggest this step, it does not cure the deficiencies of Mori. Accordingly, one ordinarily skilled in the art would not have been led to modify the references to attain the claimed subject matter.

Claims 5-11 depend on and contain all of the limitations of amended independent claim 4 and, therefore, distinguish from the references at least in the same manner as claim 4.

Moreover, there are separate grounds for patentability of amended dependent claims 6-11 which are directed to the preferred specific temperature profiles of the heating step and the reflow soldering step (claims 6, 8, 10) and the preferred specific duration for each of the heating step and the reflow soldering step (claims 7, 9, 11). As described in the specification (pg. 12), these preferred specific values for the temperature profiles and duration of the heating step and the reflow soldering step prevent deterioration of the performance of the capacitor.

While acknowledging that the combined teachings of Mori and Kurz do not disclose the specific values for the temperature profiles and duration of the heating step and the reflow soldering step recited in claims 6-11, the Examiner contends that use of such specific values "would have been logical" in order "to obtain capacitors capable of withstanding the reflow temperature without excessive heating resulting in low yield." Applicants respectfully disagree with the Examiner's contention.

In order to support a claim rejection based upon obviousness under 35 U.S.C. §103, the Examiner must provide an evidentiary basis establishing the obviousness of each modification. The Examiner may do this by citing a reference which directly establishes this obviousness, or, the Examiner may otherwise set forth a line of reasoning consistent with and motivated by the cited art establishing that such modifications would have been obvious. Mere speculation or conclusory allegations are simply inadequate to meet this burden. There must be some teaching, reason, suggestion, or motivation found in the prior art references to make a combination which renders an invention obvious within the meaning of 35 U.S.C §103. See, e.g., Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 982, 989, 18 USPQ2d 1885 (Fed. Cir. 1991).

In order to set forth a prima facie case of obviousness, the Examiner must not only demonstrate that this teaching exists in the prior art, but that it would teach all limitations of the claim. This burden cannot be met by citing references that, even if combined, fail to teach explicitly recited limitations.

Stated otherwise, in rejecting a claim as obvious under 35 U.S.C. §103, the Examiner cannot simply rely on a combination of references that teach some limitations of the claim, and make mere conclusory allegations that the combination teaches others as well.

In the instant case, the Examiner has not met his burden of establishing a prima facie case of obviousness as discussed above.

As noted by the Court of Appeals for the Federal Circuit in the case of In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992):

> 'Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so.' Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious 'modification' of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art

suggested the desirability of the modification. Wilson and Hendrix fail to suggest any motivation for, or desirability of, the changes espoused by the Examiner and endorsed by the Board.

Here, the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'

As further noted by the Federal Circuit in In re Oeticker, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992):

The prima facie case is a procedural tool of patent examination, allocating the burdens of going forward as between examiner and applicant. In re Spada, 911 F.2d 705, 707 n.3, 15 USPQ2d 1655, 1657 n.3 (Fed. Cir. 1990). The term 'prima facie case' refers only to the initial examination step. In re Piasecki, 745 F.2d1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). As discussed in In re Piasecki, the examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a prima facie case of unpatentability. If that burden is met, the burden of coming forward with evidence or argument shifts to the applicant.

* * *

If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of the patent. See In re Grabiak, 769, F.2d 729,

> 733, 226 USPQ 870, 873 (Fed. Cir. 1985); In re Rinehart, supra.
>
> In reviewing the examiner's decision on appeal, the Board must necessarily weigh all of the evidence and argument. An observation by the Board that the examiner made a prima facie case is not improper, as long as the ultimate determination of patentability is make on the entire record. In re Piasecki, 745 F.2d at 1472, 223 USPQ at 788; In re Rinehart, 531 F.2d at 1052, 189 USPQ at 147.

The Federal Circuit has therefore made it clear that the prior art must show an incentive to modify its teachings in order to render a claim obvious. Without such an incentive, a prima facie case of obviousness cannot be made.

Similarly, as the Board stated in Ex Parte Clapp, 227 USPQ 972, 973 (BPAI 1985):

> To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly expound the modifications urged by the examiner to have been obvious.

The same situation exists here. The Examiner has not provided an evidentiary basis establishing the obviousness of his proposed modification of Mori, as modified by Kurz, in order to achieve the specific values for the temperature profiles and duration of the heating step and the reflow soldering step recited in claims 6-11. There is nothing in

the references to Mori and Kurz that would expressly or implicitly teach or suggest the modification urged by the Examiner and, therefore, the references do not directly establish this obviousness. Furthermore, the Examiner has not set forth a line of reasoning consistent with and motivated by the cited art establishing that such modification would have been obvious. The only basis for the modification urged by the Examiner in the rejection is applicants' own disclosure, and such hindsighted rejections are improper. See, for example, Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315, 1318 (Fed. Cir. 1988); In re Geiger, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987); Panduit Corp. v. Dennison Manufacturing Co., 227 USPQ 337, 343 (Fed. Cir. 1985); Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985).

In view of the foregoing, applicants respectfully request that the rejection of claims 4-11 under 35 U.S.C. §103(a) as being unpatentable over Mori in view of Kurz be withdrawn.

Claims 1 and 3 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watanabe. Applicants respectfully traverse this rejection and submit that the teachings of Watanabe do not disclose or suggest the subject matter recited in amended claims 1-3.

Amended independent claim 1 is directed to a method of producing an electrical double layer capacitor as set forth above for the rejection of claims 1-3 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Kurz.

Watanabe discloses a method in which a positive electrode, a negative electrode, an electrolyte, and a gasket are assembled together to form a non-aqueous electrolyte secondary battery. However, Watanabe does not disclose or suggest a step of heating the assembled double layer capacitor, as required by amended independent claim 1. Accordingly, one ordinarily skilled in the art would not have been led to modify the reference to attain the claimed subject matter.

Claims 2-3 depend on and contain all of the limitations of amended independent claim 1 and, therefore, distinguish from the references at least in the same manner as claim 1.

In view of the foregoing, applicants respectfully request that the rejection of claims 1-3 under 35 U.S.C. §103(a) as being unpatentable over Watanabe be withdrawn.

Applicants respectfully submit that new claims 33-55 also patentably distinguish from the prior art of record.

Claims 33 and 34-35 depend on and contain all of the limitations of amended independent claims 1 and 4,

respectively, and, therefore, distinguish from the references at least in the same manner as claims 1 and 4.

New independent claim 36 is directed to a method for producing an electrical double layer capacitor an requires the steps of assembling together components comprised of a positive electrode, a negative electrode, a non-aqueous solvent, an electrolyte containing a supporting salt, a separator, and a gasket to form an electrical double layer capacitor containing a foreign substance, and heating the assembled electrical double layer capacitor to remove at least part of the foreign substance contained in the assembled electrical double layer capacitor. No corresponding combination of steps are disclosed or suggested by the prior art of record. For example, none of the cited references discloses or suggests the step of heating the assembled electrical double layer capacitor to remove at least a substantial amount of the foreign substance contained in the assembled electrical double layer capacitor, as required by independent claim 36.

Claims 37-42 depend on and contain all of the limitations of independent claim 36 and, therefore, distinguish from the references at least in the same manner as claim 36.

New independent claim 43 is directed to a method of mounting an electrical double layer capacitor on a circuit

substrate and requires the steps of providing a circuit substrate, assembling together components comprised of a positive electrode, a negative electrode, a non-aqueous solvent, an electrolyte containing a supporting salt, a separator, and a gasket to form an electrical double layer capacitor containing a foreign substance, heating the assembled electrical double layer capacitor to remove at least some of the foreign substance contained in the assembled electrical double layer capacitor, arranging the heated assembled electrical double layer capacitor on the circuit substrate, and reflow soldering the heated assembled electrical double layer capacitor on the circuit substrate. No corresponding combination of steps are disclosed or suggested by the prior art of record. For example, none of the cited references discloses or suggests the step of heating the assembled electrical double layer capacitor, prior to the reflow soldering step, to remove at least a substantial amount of the foreign substance contained in the assembled electrical double layer capacitor, as required by independent claim 43.

Claims 44-55 depend on and contain all of the limitations of independent claim 43 and, therefore, distinguish from the references at least in the same manner as claim 43.

In view of the foregoing amendments and discussion, the application is now believed to be in condition for allowance. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: COMMISSIONER OF PATENTS & TRADEMARKS, Washington, D.C. 20231, on the date indicated below.

Bruce L. Adams
Name

_____
Signature

April 1, 2003
Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title has been amended as follows:

METHOD OF PRODUCING ELECTRICAL DOUBLE LAYER CAPACITOR AND METHOD OF MOUNTING ELECTRICAL DOUBLE LAYER CAPACITOR ON A CIRCUIT SUBSTRATE

IN THE ABSTRACT:

The original abstract has been substituted with the following new abstract:

A method for producing an electrical double layer capacitor comprising the steps of assembling together components comprised of a positive electrode, a negative electrode, a non-aqueous solvent, an electrolyte containing a supporting salt, a separator, and a gasket to form a coin- or button-type electrical double layer capacitor, and heating the assembled coin- or button-type electrical double layer capacitor.

IN THE SPECIFICATION:

Paragraph beginning at line 3 of page 1 has been amended as follows:

The present invention relates to coin (button)-type electric double layer capacitors utilizing a lithium ion-conductive non-aqueous electrolyte and comprising a substance capable of occluding and discharging lithium, metallic lithium, or an alloy thereof as a negative active material, and a substance capable of occluding and discharging lithium as the positive active material[; among them, it particularly]. The present invention also relates to an electric double layer capacitor mountable by reflow a soldering[. And] and to a method of producing the same.

Heading beginning at line 21 of page 3 has been amended as follows:

[DISCLOSURE] SUMMARY OF THE INVENTION

Heading beginning at line 9 of page 9 has been amended as follows:

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[BEST MODE FOR PRACTICING THE INVENTION]

Paragraph beginning at line 21 of page 23 has been amended as follows:

Figure 1 shows a cross section view of a coin-type electric double layer capacitor. Referring to Fig. 1, main constituents are a positive electrode canister 101, an electrically conductive adhesive material 102, a positive electrode case or molding 103 for the polarizable electrode, a negative electrode canister 104, an electrically conductive adhesive material [105] 106, a negative electrode case or molding [106] 105 for the polarizable electrode, an electrolyte 109, a separator 108, and a gasket 107. The gasket 107 was made of PPS. The polarizable electrode was prepared by mixing 80 % by weight of active carbon, 10 % by weight of an electrically conductive material, i.e., carbon black, and 10 % by weight of ethylene tetrafluoride binder, which was rolled to obtain a sheet thereof. The molding 103 for the positive electrode was 0.5 [mmt] mm in thickness and 2.0 [mmγ] mm in diameter. The molding [106] 105 for the negative electrode was 0.5 [mmt] mm in thickness and 2.0 [mmΦ] mm in diameter. The moldings 103 and [106] 105 for the positive and the negative electrodes were each adhered with the positive electrode canister 101 and the negative electrode canister 104, respectively, by using the electrically conductive adhesive materials 102 and [105] 106. After

adhering the moldings with the canisters, the units of positive electrode and negative electrode were thermally treated at a temperature of 150 °C under a vacuum of 10^{-2} Torr or lower, [respectivly.] respectively.

Paragraph beginning at line 25 of page 25 has been amended as follows:

Figure 1 shows a cross section view of a coin-type electric double layer capacitor. Referring to Fig. 1, main constituents are a positive electrode canister 101, an electrically conductive adhesive material 102, a positive electrode case or molding 103 for the polarizable electrode, a negative electrode canister 104, an electrically conductive adhesive material [105] 106, a negative electrode case or molding [106] 105 for the polarizable electrode, an electrolyte 109, a separator 108, and a gasket 107. The materials used for the gasket 107 are shown in Table 1. The polarizable electrode was prepared by mixing 80 % by weight of active carbon, 10 % by weight of an electrically conductive material, i.e., carbon black, and 10 % by weight of ethylene tetrafluoride binder, which was rolled to obtain a sheet thereof. The molding 103 for the positive electrode was 0.5 [mmt] mm in thickness and 2.0 [mmϕ] mm in diameter. The molding [106] 105 for the negative electrode was 0.5 [mmt] mm

in thickness and 2.0 [mm] mm in diameter. The moldings 103 and [106] 105 for the positive and the negative electrodes were each adhered with the positive electrode canister 101 and the negative electrode canister 104, respectively, by using the electrically conductive adhesive materials 102 and [105] 106. After adhering the moldings with the canisters, the units of positive electrode and negative electrode were thermally treated at a temperature of 150 °C under a vacuum of 10^{-2} Torr or lower, respectively.

IN THE CLAIMS:

Claims 1-11 have been amended as follows:

1. (Amended) [In a] A method for producing an [electric] electrical double layer capacitor comprising, the steps of: [a positive electrode, a negative electrode, a non-aqueous solvent, an electrolyte containing a supporting salt, a separator, and a gasket, said method comprises:]

[a step of] assembling together components comprised of a [by caulk sealing inside an electric double layer capacitor said] positive electrode, [said] a negative electrode, [said] a non-aqueous solvent, [said] an electrolyte containing a supporting salt, [said] a separator, and a [said] gasket to form a coin- or button-type electrical double layer capacitor; and

[a] heating [step] the assembled coin- or button-type electrical double layer capacitor.

2. (Amended) A method for producing an [electric] electrical double layer capacitor as claimed in [Claim 1, wherein the method comprises] claim 1; further comprising the step of welding an outer connection terminal to the assembled coin- or button-type electrical double layer capacitor [said capacitor] after the heating step.

3. (Amended) A method for producing an [electric] electrical double layer capacitor as claimed in [Claim 1,] claim 1; wherein the heating step comprises heating the assembled coin- or button-type electrical double layer capacitor at a temperature [is] in a range of [from] 180 to 300 °C.

4. (Amended) [In a] A method of mounting [method comprising arranging] an electrical [electric] double layer capacitor on a circuit substrate[, said mounting method comprises:] ,comprising the steps of:

providing a circuit substrate;

[a step of] assembling together components comprised of a [by caulk sealing inside an electric double layer capacitor said] positive electrode, [said] a negative electrode, [said] a non-aqueous solvent, [said] an electrolyte

containing a supporting salt, [said] a separator, and a [said] gasket to form a coin- or button-type electrical double layer capacitor; [and

a] heating [step; and] the assembled coin- or button-type electrical double layer capacitor;

arranging the heated assembled coin- or button-type electrical double layer capacitor on the circuit substrate; and

reflow soldering the heated assembled coin- or button-type electrical double layer capacitor on the circuit substrate.

[a step of arranging and reflow soldering said electric double layer capacitor on said circuit substrate.]

5. (Amended) A [mounting] method as claimed in [Claim 4, wherein said method] claim 4; further comprising the [comprises a] step of welding an outer connection terminal to the assembled coin- or button-type electrical double layer capacitor [said electric double layer capacitor after said assembling step].

6. (Amended) A [mounting] method as claimed in [Claim 4,] claim 4; wherein[, in the] a temperature profile of the heating step in a heating region [of from 0 to] under 150 °C[, the difference between the temperature profile with

respect to time during said heating step and the temperature profile with respect to time during said reflow soldering falls within ± 50 %.] is within a range of 50% to 150% of a temperature profile of the reflow soldering step in the heating region under 150 °C.

7. (Amended) A [mounting] method as claimed in [Claim 4,] claim 4; wherein[,] a duration of the heating step in [the] a heating region [of from 0 to] under 150°C[, the difference in time duration between the time of said heating step and the time of said reflow soldering falls within ± 50%.] is within a range of 50% to 150% of a duration of the reflow soldering step in the heating region under 150°C.

8. (Amended) A [mounting] method as claimed in [Claim 4,] claim 4; wherein[, in the] a temperature profile of the heating step in a heating region of [from] 150 to 180 °C[, the difference between the temperature profile with respect to time during said heating step and the temperature profile with respect to time during said reflow soldering falls within ± 20 %.] is within a range of 80% to 120% of a temperature profile of the reflow soldering step in the heating region of 150 to 180 °C.

9. (Amended) A [mounting] method as claimed in [Claim 4,] claim 5; wherein[, in the] a duration of the heating step in a heating region of [from] 150 to 180°C[, the difference in time duration between the time of said heating step and the time of said reflow soldering falls within ± 20%.] is within a range of 80% to 120% of a duration of the reflow soldering step in the heating region of 150 to 180 °C.

10. (Amended) A [mounting] method as claimed in [Claim 4,] claim 4; wherein[, in the] a temperature profile of the heating step in a heating region of [from] 180 to 300 °C[, the difference between the temperature profile with respect to time during said heating step and the temperature profile with respect to time during said reflow soldering falls within ± 10 %.] is within a range of 90% to 110% of a temperature profile of the reflow soldering step in the heating region of 180 to 300 °C.

11. (Amended) A [mounting] method as claimed in [Claim 4,] claim 4; wherein[, in the] a duration of the heating step in a heating region of [from] 180 to 300 °C[, the difference in time duration between the time of said heating step and the time of said reflow soldering falls within ± 10 %.] is within a range of 90% to 110% of a duration of the reflow soldering step in the heating region of 180 to 300 °C.